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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/072,959	05/05/1998	PAI HUNG PAN	2919.1US	7136

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EXAMINER
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FOURSON III, GEORGE R

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.



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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

Application Number: 09/072,959  
Filing Date: May 05, 1998  
Appellant(s): PAN, PAI HUNG

**MAILED**

**JUN 28 2004**

**GROUP 2800**

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Brick G. Power  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 4/23/04.

Art Unit: 2823

**(1) *Real Party in Interest***

A statement identifying the real party in interest is contained in the brief.

**(2) *Related Appeals and Interferences***

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

**(3) *Status of Claims***

The statement of the status of the claims contained in the brief is correct.

**(4) *Status of Amendments After Final***

No amendment after final has been filed.

**(5) *Summary of Invention***

The summary of invention contained in the brief is correct.

**(6) *Issues***

The appellant's statement of the issues in the brief is correct.

**(7) *Grouping of Claims***

The rejection of claims 1-5, 11-17, 25-28 and 33-38 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

**(8) *Claims Appealed***

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(9) Prior Art of Record**

5,712,185                                      TSAI                                      1-1998

Lee, H.S., et al, "An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI)", 1996 IEEE Symposium on VLSI Technology Digest of Technical Papers (1996), pp.158-159

**(10) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-4,11-14,16,25-27,33-35 and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsai et al.

Tsai et al discloses in figures 3a-3h and the accompanying description formation of dielectric layer 32 and buffer layer 34 over semiconductor substrate 30, patterning of layers 32 and 34, trench etching using the patterned layers 32 and 34 as a trench mask, thermal oxidation of the trench walls, selective isotropic etching of layer 34 and filling of the trench with silicon dioxide isolation material. Further, the references teaches as an alternative to the depicted process removal of layer 36A prior to deposition of the trench fill oxide (col.3, lines 33-34). In that embodiment the trench fill oxide would contact both the top major surface of the buffer layer 34 and the side surface of buffer layer 34.

Claims 17 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al as applied to claims 1-4,11-14,16,25-27,33-35 and 37 above, and further in view of the following comment.

Tsai et al discloses removal of 50-100 angstroms of buffer layer 34. In view of this disclosure, one of ordinary skill in the art would have been led to the recited amount of buffer layer 34 to be removed to

achieve formation of desired device dimensions and resulting device characteristics on the finished wafer. Further, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

Claims 5,15,28 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al as applied to claims 1-4,11-14,16,25-27,33-35 and 37 above, and further in view of Lee et al.

Tsai et al does not disclose densification of the trench fill material. Lee et al discloses densification of trench fill material (abstract, for example). It would have been within the scope of one of ordinary skill in the art to combine the teachings of the Tsai et al and Lee et al to enable the trench fill material of Tsai et al to be densified according to the teachings of Lee et al that the method is intended for trench fill dielectrics and to obtain the benefit disclosed by Lee et al of reduced oxide consumption in subsequent process steps (p.158, col.1, lines 23-25).


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**(11) Response to Argument**

Applicant argues that the side surface of buffer layer 34 is not a major surface of the layer. However, the issue is moot because the reference teaches as an alternative to the depicted process removal of layer 36A prior to deposition of the trench fill oxide (col.3, lines 33-34). In that embodiment the trench fill oxide would contact both the top major surface of the buffer layer 34 and the side surface of buffer layer 34 thereby being encompassed by the recitation of contacting a major surface of the layer 34.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

  
George Fourson  
Primary Examiner  
Art Unit 2823

George Fourson  
June 28, 2004

Conferees

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